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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,597	10/01/2003	Peter Beer	W&B-INF-1951	7989

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LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
YOHA, CONNIE C	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,597	BEER, PETER	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The response filed on 3/25/05 has been entered and are made of record.

2. Claims 1-5 are pending.

3. Claim 1-5 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Frankowsky et al, Pat. No. 6608783.

The reason for this rejection has been set forth in the previous action and is also disclosed in this action.

Claim Rejections - 35 USC э 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Frankowsky et al, Pat. No. 6608783.

With regard to claim 1, Frankowsky discloses a memory circuit, comprising: a memory cell array (fig. 4, 10) including a plurality of memory cells (fig. 4, M1-M8), said memory cell array including a plurality of word lines (fig. 4, WL0-WL7) and a plurality of bit lines (fig. 4, BL0-BL7) for addressing said plurality of memory cells (col. 4, line 5-15); a plurality of write amplifiers (fig. 4, SA0-SA3) for writing to the plurality of memory cells (col. 2, line 38-42 and col. 3, line 1-4, especially stated that data are fed to (meaning

write to) the sense amplifier to the memory cells in accordance with the invert/non-inverted signals produced by the address logic.), each one of the plurality of write amplifiers assigned to a group of said plurality of bit lines (fig. 4, BL0-BL7) (col. 4, line 10-15); an address decoding circuit (fig. 6, column decoder) for simultaneously activating a group of said plurality of write amplifiers (col. 6, line 17-60, where Frankowsky disclosed that his device is capable of operating in a multi bank operation. Each of the sense amplifier from each bank (making them a plurality of sense amplifier) are being activated simultaneously as the multiple banks of the entire array are in operation. When in test mode, the write data (inverted or non-inverter) are written into the corresponding banks (according to the banks address and column and row address) through the write amplifiers simultaneously, depending on a test mode signal (fig. 4, TEST MODE), so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of said plurality of bit lines (col. 4, line 62-col. 5, line 18) (col. 6, line 17-60).

With regard to claim 2, Frankowsky discloses further a plurality of switching devices (fig. 4, 17); each one of the plurality of write amplifiers connected to assigned ones of said plurality of bit lines via a respective one of said plurality of switching devices (fig. 4, DI0-DI3) in order to write the test datum from an activated one of said plurality of write amplifiers to an addressed memory cell via one of said plurality of bit lines addressed by a write address (col. 4, line 50-61).

With regard to claim 3, Frankowsky discloses wherein said address decoding circuit (fig. 4, 12) is configured to simultaneously connect one of said plurality of write

amplifiers to assigned ones of said plurality of bit lines depending on the test mode signal (fig. 4, TEST MODE) (col. 4, line 62-col. 5, line 18).

Drafted as Method claim

5. As per claim 4-5 encompass the same scope of invention as to that of claim 1-3 except they are draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Response to Arguments

6. Applicant's arguments filed 3/25/05 have been fully considered but they are not persuasive.

In response to the applicant's argument concerning the patentable difference between the subject mater of claims 1 and 4 of the instant application and Frankowsky are disagreed by the examiner.

Applicant argued that Frankowsky does not teach the write amplifiers by which the write data is to be driven to the bit lines. Applicant argued that the sense amplifiers SA0-SA3 of Frankowsky is used for reading out data from the memory array only and therefore they are not write sense amplifier as claimed in the instant invention. Examiner disagreed with this statement. Frankowsky discloses that his sense amplifier SA0-SA3 can be a read sense amplifier or a write sense amplifier depending on the mode of operation (write or read portion of a test mode). As a read sense amplifier,

data are read out and as a write sense amplifier, data are fed to the sense amplifier (see col. 2, line 38-42) (col. 3, line 1-4) (col. 5, line 1-28). Examiner likes to redirect the applicant to **column 5, line 1-8**, where Frankowsky clearly disclosed that during the **write portion of the test mode**, the write data (whether it is inverted or non-inverter data) are being passed from the I/O terminal to the sense amplifier SA0 of which the sense amplifiers are now operate as write amplifiers, feeding (or writing) the data from the I/O terminal to the memory array cells. Therefore, Frankowsky does disclose a plurality of write amplifiers (fig. 4, SA0-SA3) for writing to the plurality of memory cells as claimed in the instant invention.

With regard to the argument that Frankowsky does not disclose that the address logic is able, depending on a test mode signal, to simultaneously activate a group of write amplifiers so that the write amplifiers drive the applied test data to the corresponding bit lines as recited in claim 1 and 4 of the instant application. Examiner disagrees with this argument. Examiner likes to redirect the applicant to column 6, starting at line 17-60, where Frankowsky disclosed the memory device is capable of operating in a multi bank operation. Each of the sense amplifier from each bank (making them a plurality of sense amplifier) are being activated simultaneously as the multiple banks of the entire array are in operation. When in the test mode, the write data (inverted or non-inverter) are written into the corresponding banks (according to the banks address and column and row address) through the write amplifiers simultaneously. Therefore, Frankowsky does disclose the address decoding circuit (fig. 6, column decoder) corresponding to the column address CA and bank BA for

simultaneously activating a group of plurality of write amplifiers (fig. 6, sense amplifier SA0-SA3 from bank A, B, C, D), depending on a test mode signal (fig. 6, TEST MODE) as claimed in claim 1 and 4 or the instant invention.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone

number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.Yoha

June 2005

CONNIE C. YOHA
PRIMARY EXAMINER